Bit assignment of the RC memory word (32+6 bits) of the Heating TX radar controller

Bit N:o	Signal	Direction	Description	Default		Destination
	LPRPint		Not programmable			
61	Spare		HB5	0		
60	Spare		HB4	0		
59	Spare	NOT USET	HB3	0	0	
58	Spare		HB2	0		
57	Spare		HB1	0		
56	Spare		HB0	0		
31	TXSYNC			0		Front panel PNC
30	RFC2	O, 0 active	TX 3/4 ON	1	7	SOUSY switch
29	RFC3	O, 0 active	TX 5/6 ON	1		SOUSY switch
28	RFC4	O, 0 active	TX 7/8 ON	1		SOUSY switch
27	RFC5	O, 0 active	TX 9/10 ON	1		SOUSY switch
26	RFC6	O, 0 active	TX 11/12 ON	1	F	SOUSY switch
25	FLP1	O, 0 active	Phase flip 180 TX 1/3	1		SOUSY switch
24	FLP2	O, 0 active	Phase flip 180 TX 2/4	1		SOUSY switch
23	FLP3	O, 0 active	Phase flip 180 TX 5/7	1		SOUSY switch
22	FLP4	O, 0 active	Phase flip 180 TX 6/8	1	F	SOUSY switch
21	FLP5	O, 0 active	Phase flip 180 TX 9/11	1		SOUSY switch
20	FLP6	O, 0 active	Phase flip 180 TX 10/12	1		SOUSY switch
19	TRSW	O, 1 active		0		SOUSY switch
18	RFC1	O, 0 active	TX1/2 ON	1	7	SOUSY switch
17	RXP1B	O, ?	Receiver protector bit B	1		RX-protector 1B
16	RXP1A	O, ?	Receiver protector bit A	1		RX-protector 1A
15	PS1	O	Prof select bit 1 (common to all DDS)	0		all DDS boards
14	PS0	O	Prof select bit 0 (common to all DDS)	0	3	all DDS boards
13	STMC7	O, neg. pulse	Start modul. counter to DDS t11 and t12	1		DDS board 6
12	STMC6	O, neg. pulse	Start modul. counter to DDS t9 and t10	1		DDS board 5
11	STMC5	O, neg. pulse	Start modul. counter to DDS t7and t8	1		DDS board 4
10	STMC4	O, neg. pulse	Start modul. counter to DDS t5 and t6	1	F	DDS board 3
9	STMC3	O, neg. pulse	Start modul. counter to DDS t3 and t4	1		DDS board 2
8	STMC2	O, neg. pulse	Start modul. counter to DDS t1 and t2	1		DDS board 1
7	STMC1	O, neg. pulse	Start modul. counter to DDS m1 and m2	1		DDS master
6	UPD7	O, pos. pulse	I/O-update to DDS modules t11 and t12	0	8	DDS board 6
5	UPD6	O, pos. pulse	I/O-update to DDS modules t9 and t10	0		DDS board 5
4	UPD5	O, pos. pulse	I/O-update to DDS modules t7 and t8	0		DDS board 4
3	UPD4	O, pos. pulse	I/O-update to DDS modules t5 and t6	0		DDS board 3
2	UPD3	O, pos. pulse	I/O-update to DDS modules t3 and t4	0	0	DDS board 2
1	UPD2	O, pos. pulse	I/O-update to DDS modules t1 and t2	0		DDS board 1
0	UPD1	O, pos. pulse	I/O-update to DDS modules m1 and m2	0		DDS master
	PatchClk *)	O, pos. pulse	Strobes the RC register, on DDS boards			
	LPRPint		Last Pulse Repetition Period interrupt from R/C HW			
	PatchClk		Timing Clock, from R/C HW			
	Running		R/C running, from R/C HW			

1) Pins are defined in the RC pin assignment document (rows P2 a1-a32 and P2 c1- c32).
*) Separate signal from the RC.

O =output

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