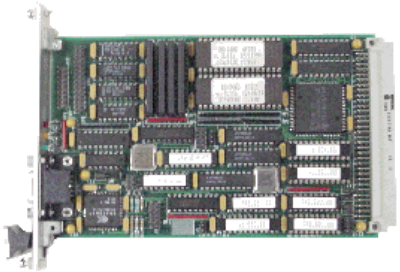
An introduction to VMEbus

Overview

- What you already should know
- VMEbus
  - Introduction
  - Addressing
  - Single cycles
  - Block transfers
  - Interrupts
  - VME64x
- System assembly
- Single Board Computer
- Software
- Tools

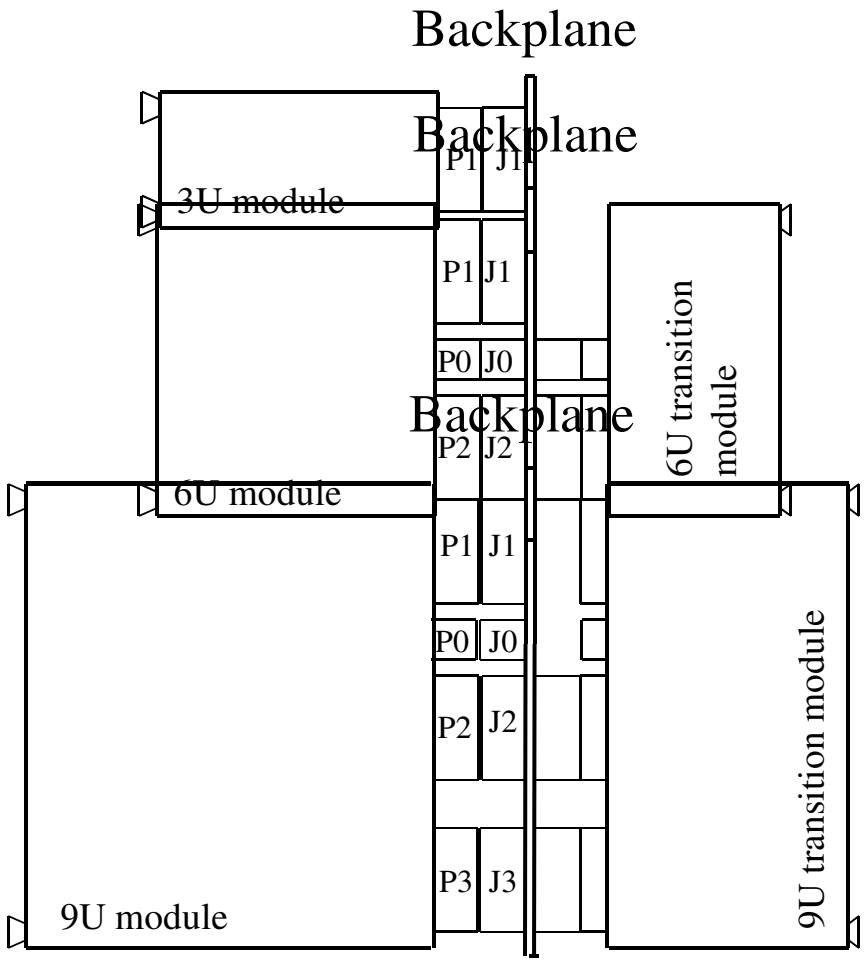
VMEbus mechanics

VMEbus cards exist in 3 standard heights: 3U, 6U and 9U
Definition: 1U = 1.75 inch



In 6U and 9U systems there can be transition modules installed on the rear side of the backplane. Transition modules do not connect to VMEbus but just to the VMEbus module on the opposite side of the backplane via the user defined pins of the J0, J2 and J3 connectors

VMEbus mechanics (2)



VMEbus mechanics (3)

Example: 6U VME64x module

Alignment pin
Incompatible with certain old crates

Insertion force
(415 pins * 1 N)

5 row P1 connector
160 pins used for VMEbus

P0 connector
Used for PMC I/O
Incompatible with certain crates
(Jaux, VME64xP)

Injector / extractor handles
Push red button

5 row P2 connector
32 pins used for VMEbus
Other pins user defined (e.g. for transition modules)

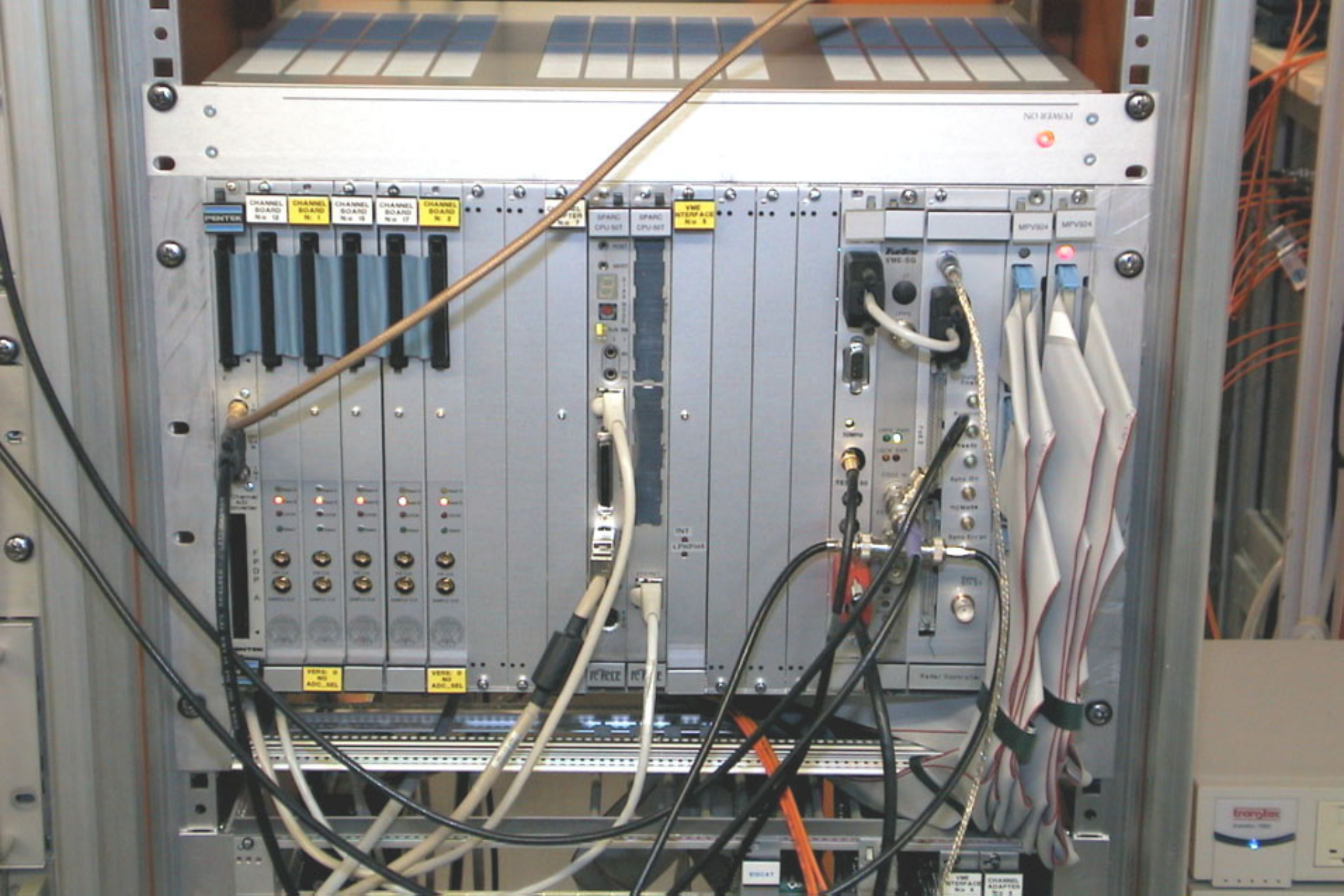
Discharge strip

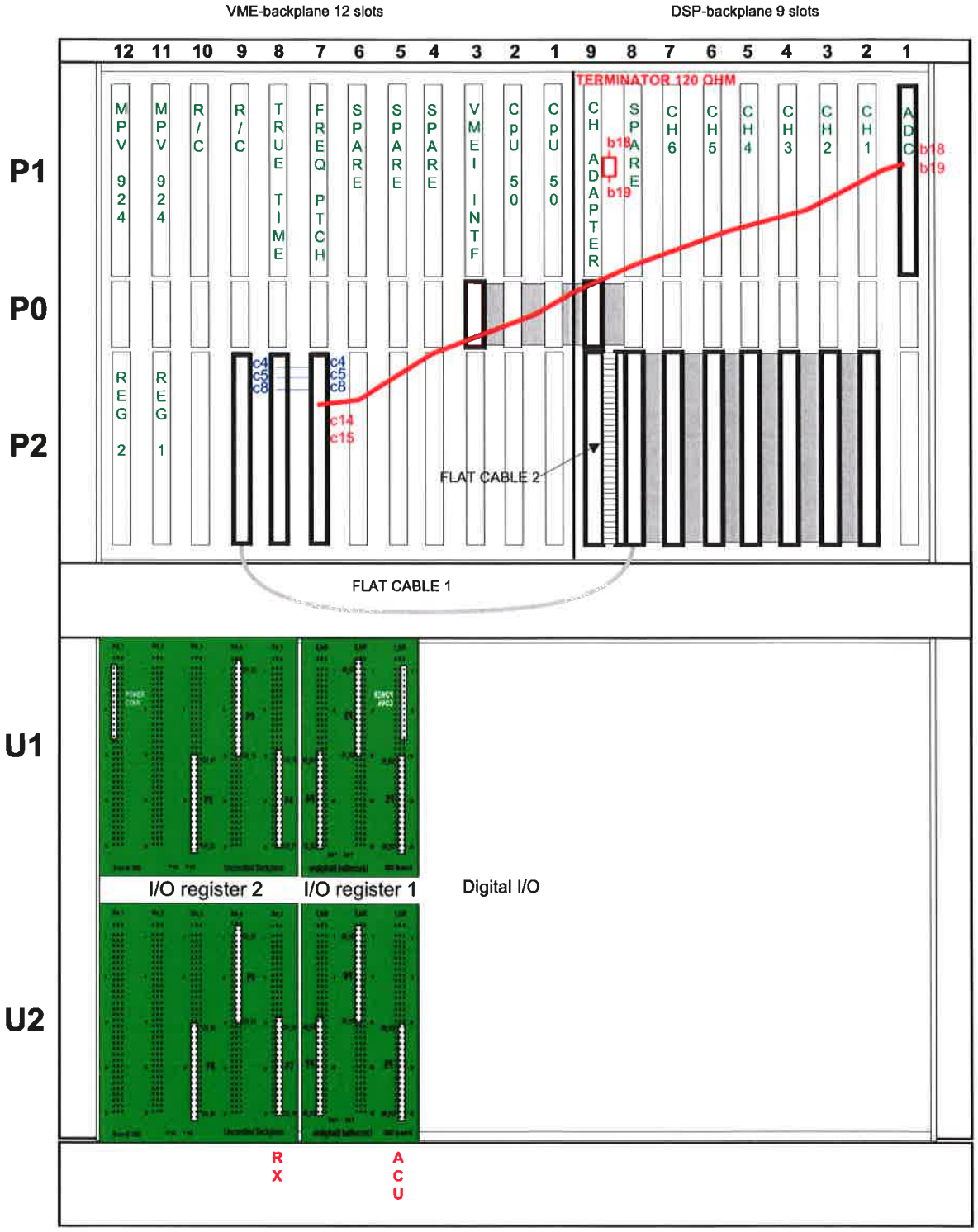
VMEbus crates

21 slot 6U crate
for 19” racks

21 slot 9U crate
(with 6U section)
for 19” racks

- There are different types of power supplies (5V, +/- 12V, 3.3V, 48V) mounted locally or remote
- The fan-tray unit allows to monitor parameters like voltages, currents, fan speed, temperature
- (Some) crates can be controlled by a field bus (CAN)
- ATTENTION: The EMC gasket to the left of slot 1 may damage your VMEbus cards


CHANNEL BOARD
SPARC CPU-SIT
VME INTERFACE
MPV924

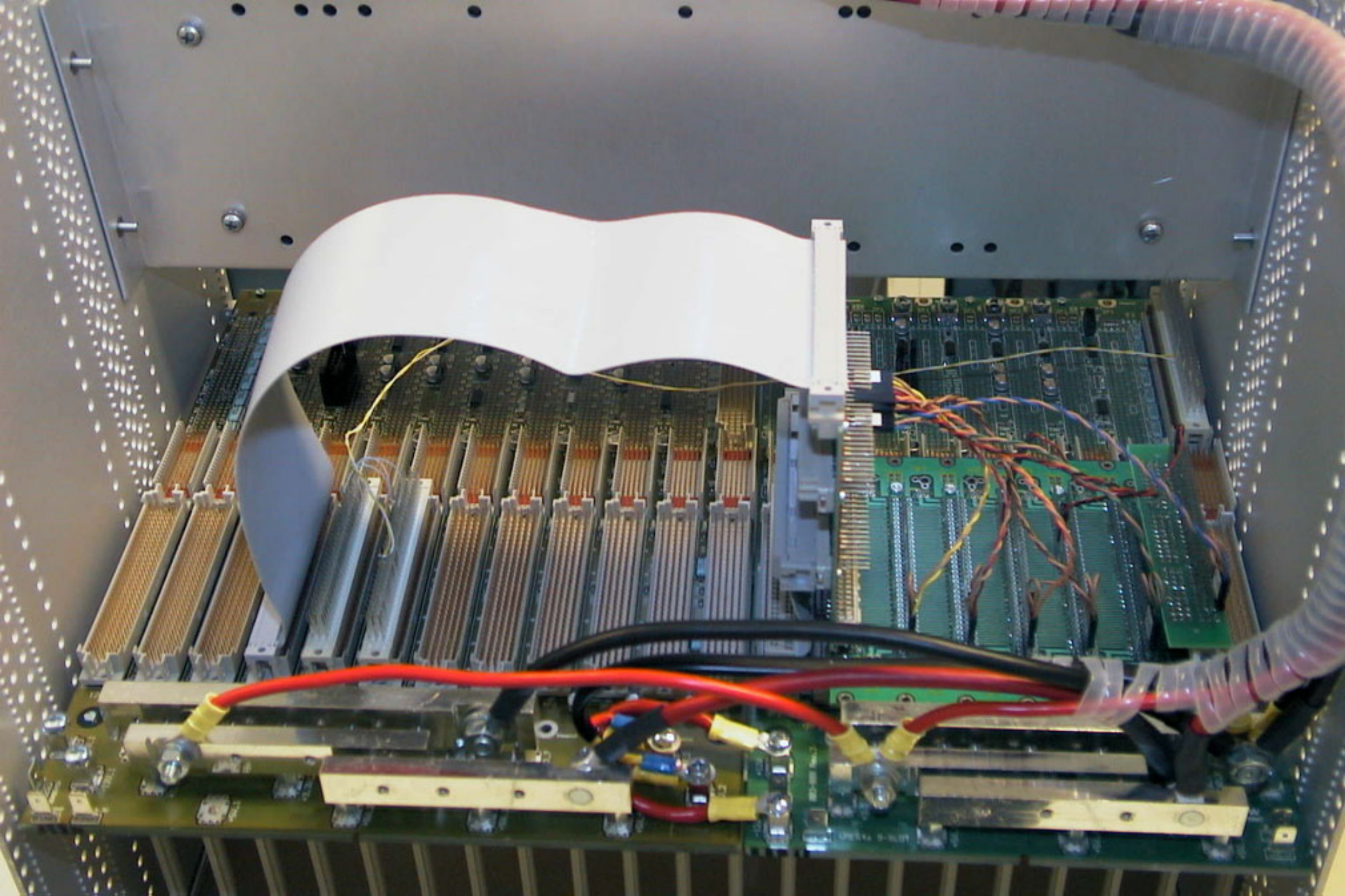


Firelist:

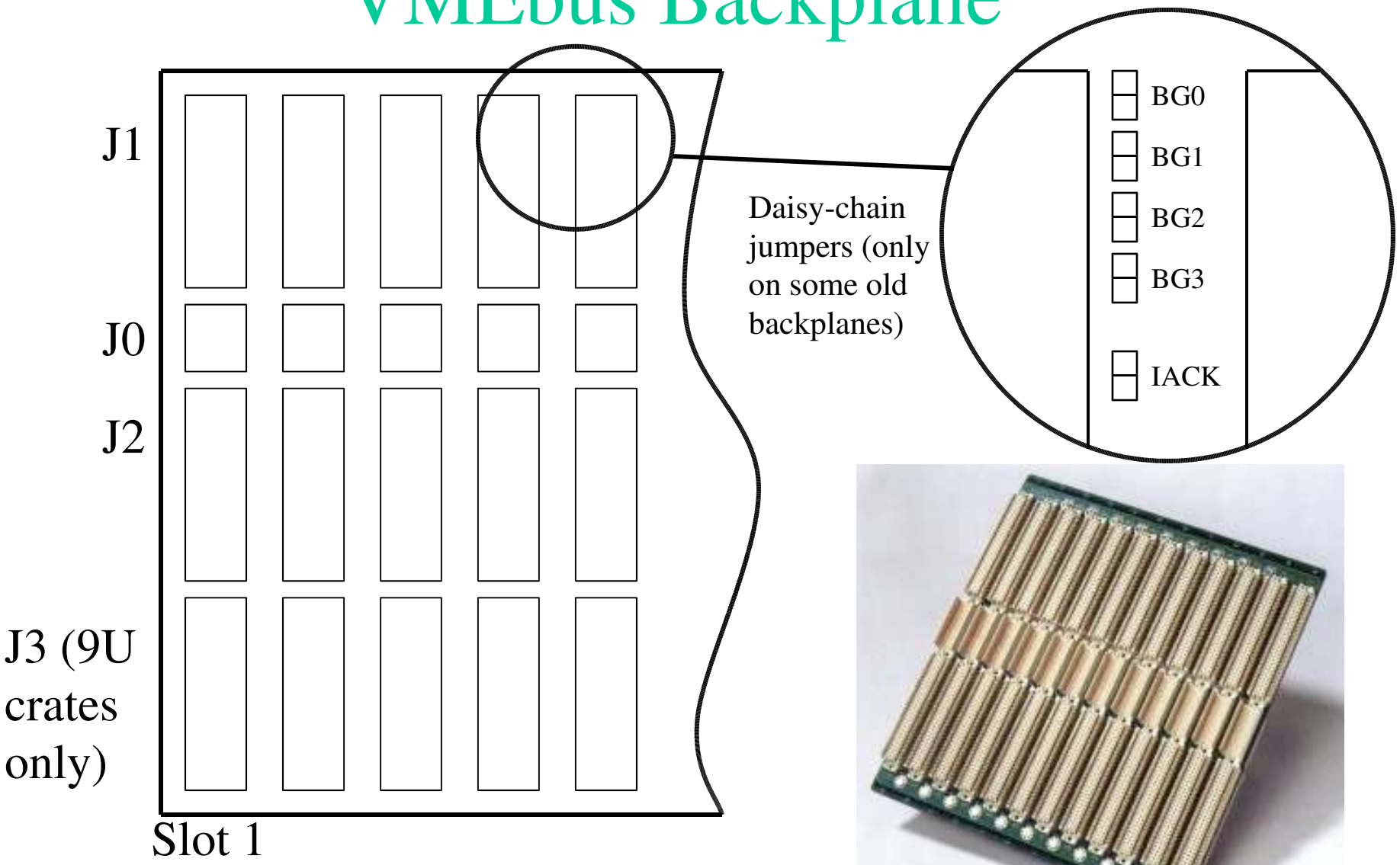
P2 9 c4 to P2 7 c4
P2 9 c5 to P2 7 c4
P2 9 c6 to P2 7 c6
P2 7 c14 to E1 1 b18
P2 7 c15 to E1 1 b19

Backplane E1 modification:

E1 b18 and E1 b19 terminations of these lines are moved at the both ends (slot 1 and 9).
At slot 9 resistor 120 ohms is connected between lines b18 and b19 (cross).



VMEbus Backplane



6U VME64x backplane

VMEbus basics

- Electrical properties
  - All lines use TTL levels
  - Low = 0 ... 0.6 V
  - High = 2.4 ... 5 V
  - Address, address modifier and data lines are active high
  - Protocol lines are active low
- Protocol
  - Asynchronous with 4-edge handshaking.
  - The duration of a VMEbus cycle depends on the speed of the master and the slave
- Byte ordering
  - VMEbus is big endian. It stores the most significant byte of a word at the lowest byte address (0x0)
  - PCI and Intel CPUs are little endian. They store the most significant byte of a word at the highest byte address (0x3)
  - Most VMEbus masters (e.g. VP110) have automatic byte swapping logic

VMEbus basics(2)

- Types of common modules (physical and logical)
  - Master
    - A module that can initiate data transfers
  - Slave
    - A module that responds to a master
  - Interrupter
    - A module that can send an interrupt (usually a slave)
  - Interrupt handler
    - A module that can receive (and handle) interrupts (usually a Single Board Computer)
  - Arbiter
    - A piece of electronics (usually included in the SBC) that arbitrates bus access and monitors the status of the bus. It should always be installed in slot 1 of the VMEbus crate

VMEbus basics(3)

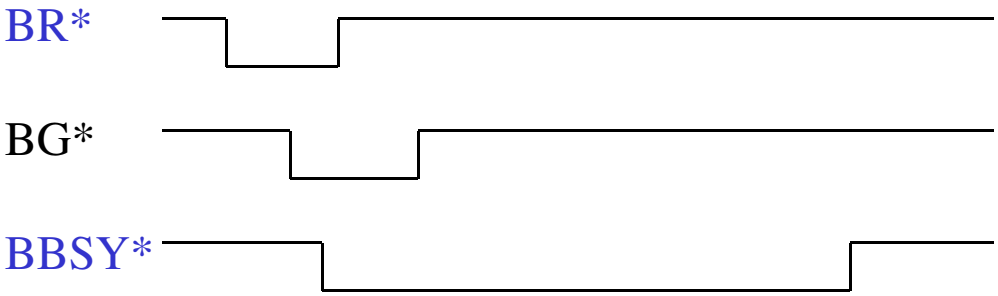
- Main types of data transfers
  - Single cycles
    - Transfer 8, 16 or 32 bits of data (typically) under the control of the CPU on the master
    - Typical duration: 1 us
  - Block transfer (DMA)
    - Transfer any amount of data (usually 32 or 64 bit at a time) under the control of a DMA controller (CPU independent)
    - Data is transferred in bursts of up to 256 (D32) or 2048 (D64) bytes
    - Typical duration: 150 ns per data word
  - Interrupts
    - Used typically by slaves to signal a condition (e.g. data available, internal error, etc.)
    - Can (in principle) have 7 priorities
    - The interrupter provides an 8-bit vector on request of the interrupt handler to identify itself
    - ROAK (Release on Acknowledge) or RORA (Release On Register Access)

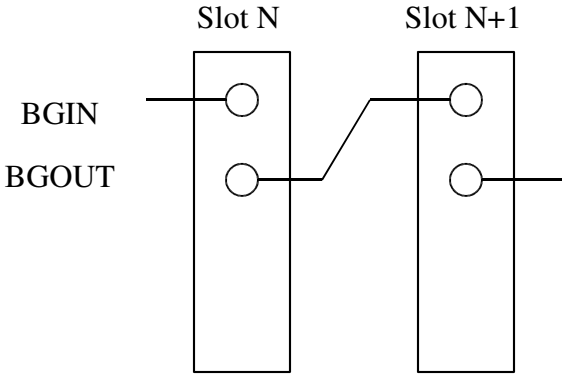
Important signals

Name	Description
BBSY*	Bus Busy. Once a master has been granted the bus it drives BBSY*. As long as BBSY* is asserted no other master can get the bus
A[31..1]	Address lines (can carry data in D64 multiplexed transfers)
D[31..0]	Data lines
AM[5..0]	Address modifier. Defines the number of valid address bits and cycle type
DS0* and DS1*	Data strobes. Tell the slave when the master is ready. Also encode the number of bytes to be transferred
LWORD*	Contributes to the definition of the transfer size and carries data in MBLT cycles
AS*	Address Strobe. Tells the slaves when the address on the bus is valid
WRITE*	Defines the direction of the data transfer
DTACK*	Data acknowledge. Used by a slave to tell the master that it has read / written the data
BERR*	Bus error. Used by slaves or arbiters to signal errors
IRQ1* .. IRQ7*	Interrupt request lines. Asserted by the interrupter
IACK*	Interrupt acknowledge. Used by the interrupt handler to retrieve an interrupt vector from the interrupter

Arbitration

- Before a master can transfer data it has to request the bus. It does this by asserting one of the four bus request lines
  - The lines (BR0, BR1, BR2 and BR3) can be used to prioritize requests in multi-master systems
- The arbiter (usually in slot 1) knows (by looking at the BBSY line) if the bus is busy or idle. Once it is idle it asserts one of the four Bus Grant out lines (BGOUT 0..3)
- If a master detects a 1 on the BGIN line corresponding to its BR it claims the bus by asserting BBSY (otherwise it passes BGIN on to BGOUT to close the daisy chain)





Color code: Arbiter - Master

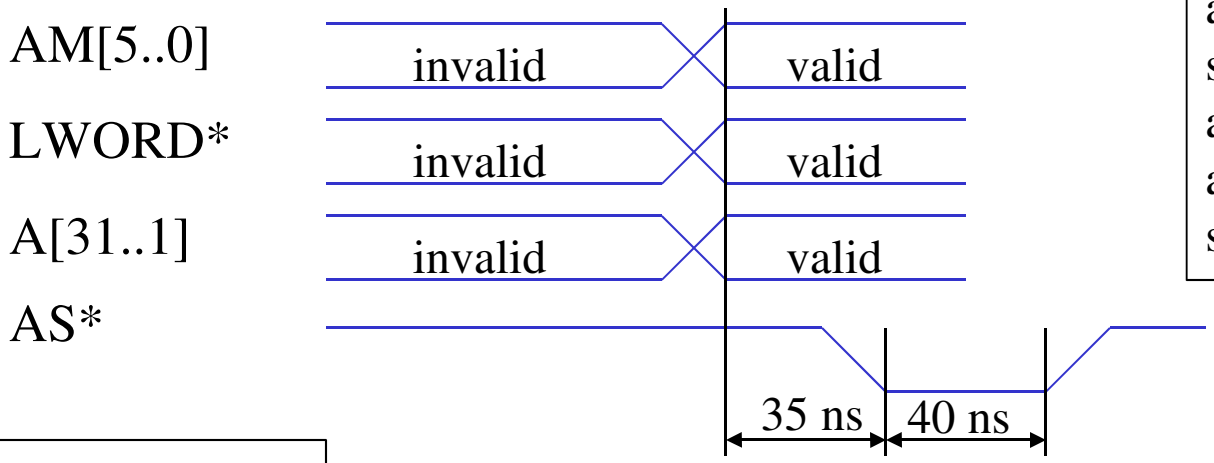
Addressing

- The VMEbus backplane has 31 address lines: A01..A31
- There is no A00 address line on the backplane. This information is encoded in the DS0/1 protocol lines
- A slave is selected by two criteria:
  - Address (usually 16, 24 or 32 valid bits)
  - Address modifier (6 bits). It defines:
    - The number of valid address bits
    - The access mode (user/supervisor, program/data, CR/CSR)
    - The transfer type (single cycle or block transfer)
- Typically slaves respond to only one address width (A16, A24 or A32; read the manual of the slave) but may allow both single cycles and block transfers
- The base address of a slave can be set:
    - Mechanically: on-board Jumpers, DIP switches
    - By S/W: VME64x geographical addressing, CR/CSR

Addressing protocol

- First the master drives AM, Address and LWORD*. Then it waits 35 ns and finally drives AS* to validate the information
- The slave has to decode the address information within 40 ns (even though most masters keep AS* asserted much longer)
- The master does not know if a slave has accepted the address information. It continues with the data transfer until it either receives a DTACK* or a BERR*
- If two or more slaves believe to be addressed you have a problem…

The timing parameters mentioned here are two of about 50 in the VMEbus standard. The standard also distinguishes master and slave timing (bus skew)



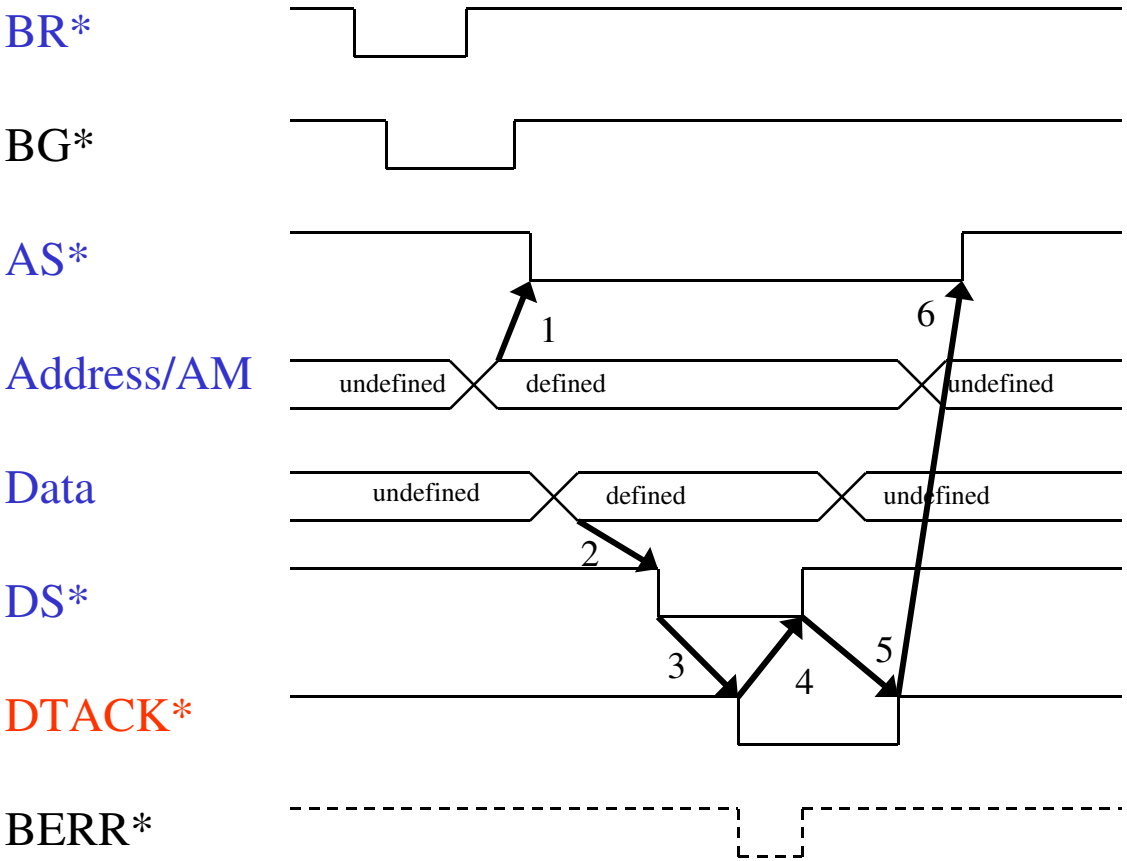
Color code: Master

(Common) VMEbus AM codes

AM code	Description
0x08	A32, user, 64-bit (MBLT) block transfer
0x09	A32, user, data, single cycle
0x0A	A32, user, program, single cycle
0x0B	A32, user, 32-bit (BLT) block transfer
0x0C	A32, supervisor, 64-bit (MBLT) block transfer
0x0D	A32, supervisor, data, single cycle
0x0E	A32, supervisor, program, single cycle
0x0F	A32, supervisor, 32-bit (BLT) block transfer
0x29	A16, user, data, single cycle
0x2C	A16, supervisor, data, single cycle
0x2F	CR/CSR single cycle (geographical addressing)
0x38	A24, user, 64-bit (MBLT) block transfer
0x39	A24, user, data, single cycle
0x3A	A24, user, program, single cycle
0x3B	A24, user, 32-bit (BLT) block transfer
0x3C	A24, supervisor, 64-bit (MBLT) block transfer
0x3D	A24, supervisor, data, single cycle
0x3E	A24, supervisor, program, single cycle
0x3F	A24, supervisor, 32-bit (BLT) block transfer

Single cycles

Example: (Simplified) write cycle



1: Master drives address and AM code. Then it asserts AS
2: Master puts data on the bus. Then it asserts DS
3: Slave latches data and drives DTACK
4: Master removes DS
5: Slave removes DTACK
6: Master releases Address, AM and data lines. Then it releases AS

Color code: Master - Slave - Arbiter

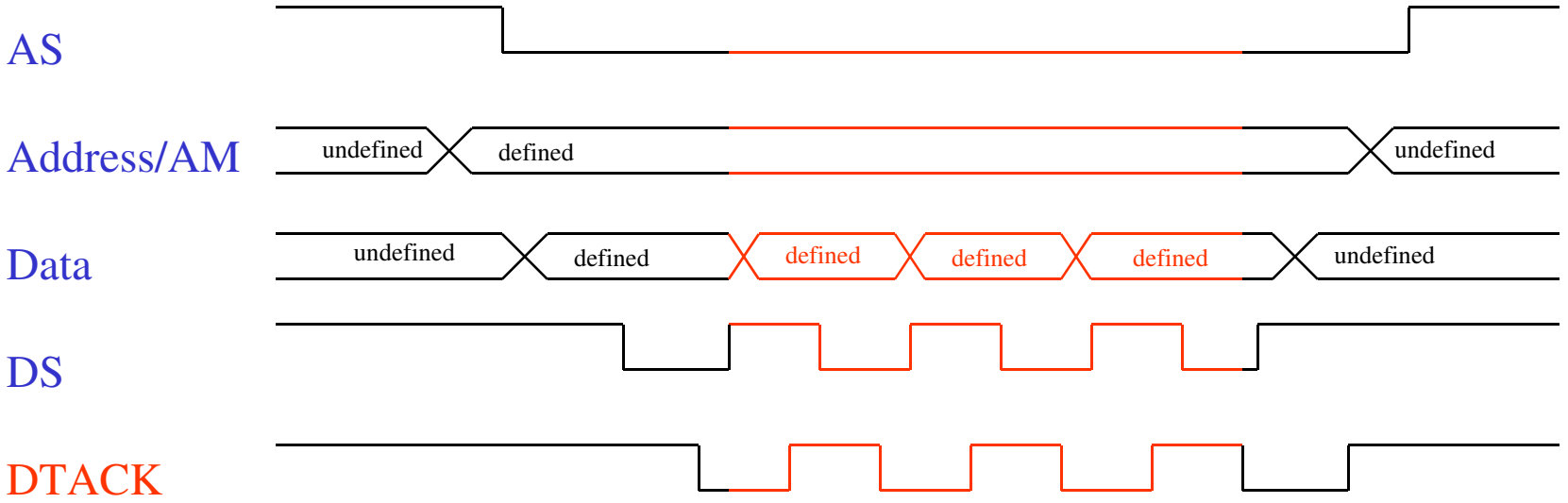
Single cycles (2)

- The number of bytes to be transferred (1, 2 or 4) is encoded in the DS0, DS1 and LWORD protocol lines
- Remember that some slaves support only certain data widths (e.g. D8 and D16 but not D32)
- The VMEbus address should be aligned to the data size
  - Reading a D32 word e.g. from address 0x000003 may not be a good idea
- VMEbus also supports (rarely used) read-modify-write cycles (useful for semaphores)
- Remember that VMEbus is big endian. Example:

Address	Action	Result
0x00000000	D32 write 0x11223344	--
0x00000000	D32 read	0x11223344
0x00000000	D8 read	0x11
0x00000003	D8 read	0x44

Block transfers

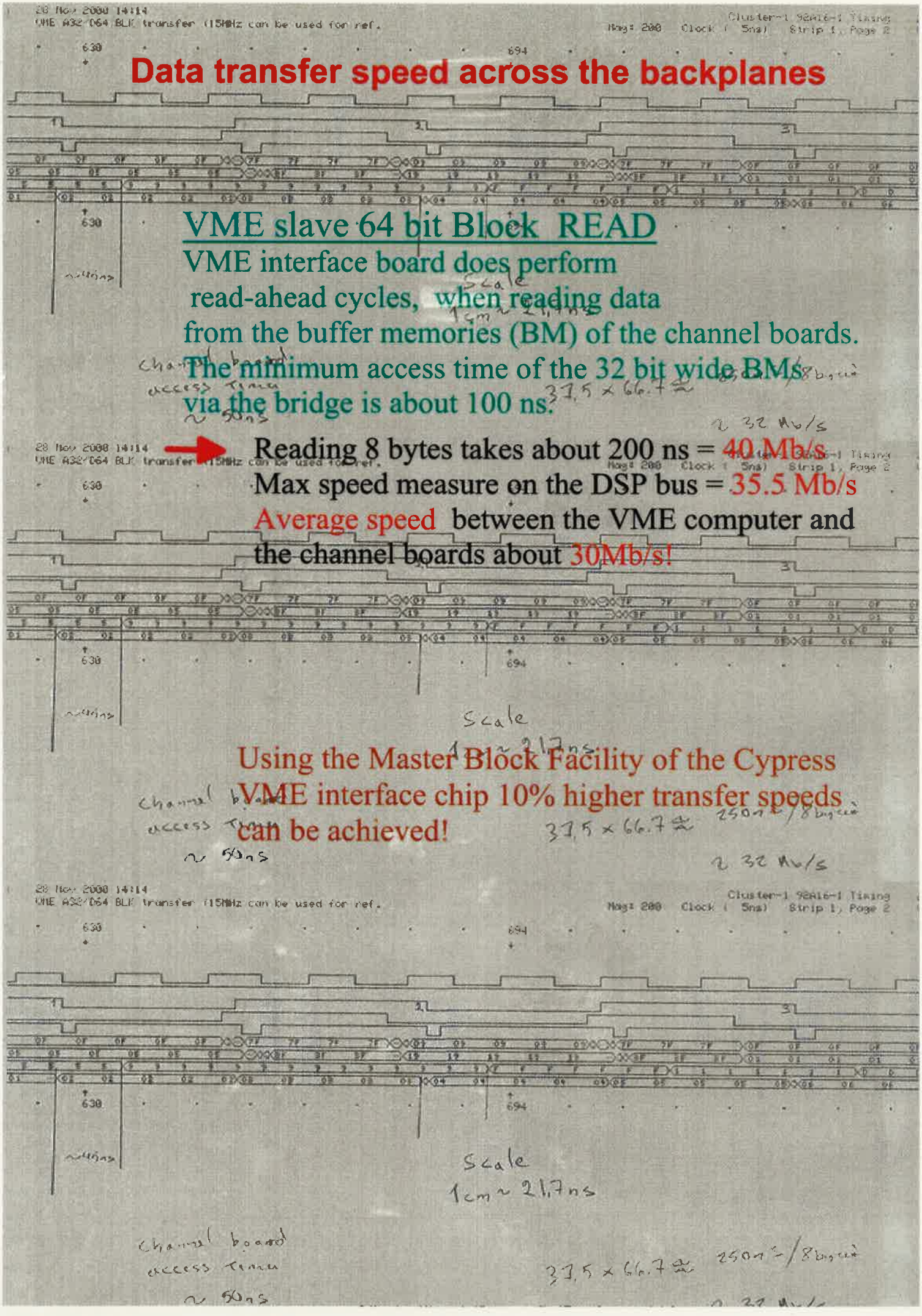
Example: D32 write



- The Block transfer protocol is based on the single cycle protocol
- The address lines on the backplane do not change state during the transfer. Both master and slave use internal counters to keep track of the address
- As the address lines are not used they can carry data: 64-bit multiplexed DMA. In this case the slave uses DTACK for two purposes:
  - Directly after AS being asserted to acknowledge the address
  - After each assertion of DS to acknowledge the data

Color code: Single cycle protocol – block transfer

Data transfer speed across the backplanes



VME slave 64 bit Block READ

VME interface board does perform read-ahead cycles, when reading data from the buffer memories (BM) of the channel boards.

The minimum access time of the 32 bit wide BMs via the bridge is about 100 ns.

→ Reading 8 bytes takes about 200 ns = 40 Mb/s

Max speed measure on the DSP bus = 35.5 Mb/s

Average speed between the VME computer and the channel boards about 30Mb/s!

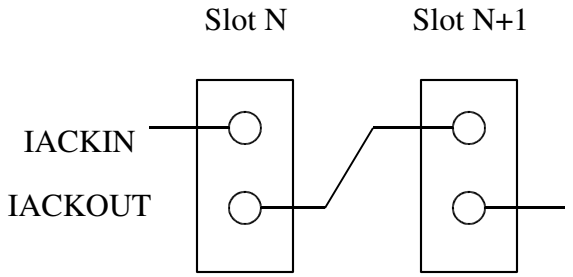
Using the Master Block Facility of the Cypress VME interface chip 10% higher transfer speeds can be achieved!

VMEbus typical performance

- Being a handshaked, asynchronous protocol there is no fixed transfer rate such as for e.g. RS232. The timing parameters (see VMEbus standard) however set an upper limit.
- Single cycles: Typical performance = 1 µs per transfer
  - D8 = 1 MB/s
  - D16 = 2 MB/s
  - D32 = 4 MB/s
- **Write posting** decouples PCI and VMEbus cycle. This increases the performance to ~ 10 MB/s for D32 
- Block transfers
  - D32 = 20..25 MB/s (theoretical: 40 MB/s)
  - D64 = 40..50 MB/s (theoretical: 80 MB/s)

Interrupts

- VMEbus provides 7 interrupt levels (= bus lines) to prioritize interrupts
- Each interrupter can use any level
- There must only be one interrupt handler for each level
- The interrupt handler uses (under H/W control) a special type of single cycle (IACK cycle) to obtain an 8-bit vector from the interrupter. This vector (set by jumpers or S/W) must be unique (within the crate) and identifies the source of the interrupt
- There are two types of interrupters:
  - ROAK (preferred)
    - The IACK cycle clears the interrupt
  - RORA
    - The interrupt is cleared by an additional register access (single read or write cycle)
- Typically an interrupt gets handled by the H/W in a few µs (once the VMEbus is free). There can be additional (possibly large) S/W overheads depending on the operating system used and the state of the CPU
- If two interrupters are active at the same time and on the same level the one closer to slot 1 will be serviced first (IACK daisy chain)

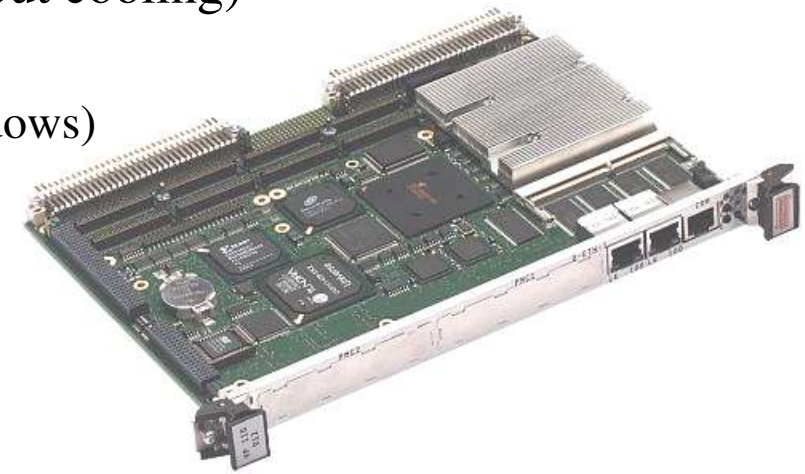


VME64x

- VME64x is a set of extensions to the VMEbus standard made in 1997
- Most features are optional and fall into one of four categories:
  - Mechanics
    - 5-row P1/J1 and P2/J2 connectors
    - J0/P0 connector
    - Alignment pin
    - EMC gaskets
    - Injector / extractor handles
    - Discharge strips
    - Card keys
    - Solder side covers
  - Plug-and-play
    - Geographical addressing (access a module by its slot number)
    - CR/CSR space: Standardised registers for the automatic configuration of a module (base address(es), interrupt vector(s), etc.)
  - Power
    - 3.3 V and 48 V
    - Additional 5 V
  - 2eVME Protocol: A rarely used way of speeding up block transfers (theoretical bandwidth: 160 MB/s)

The VMEbus single board computer

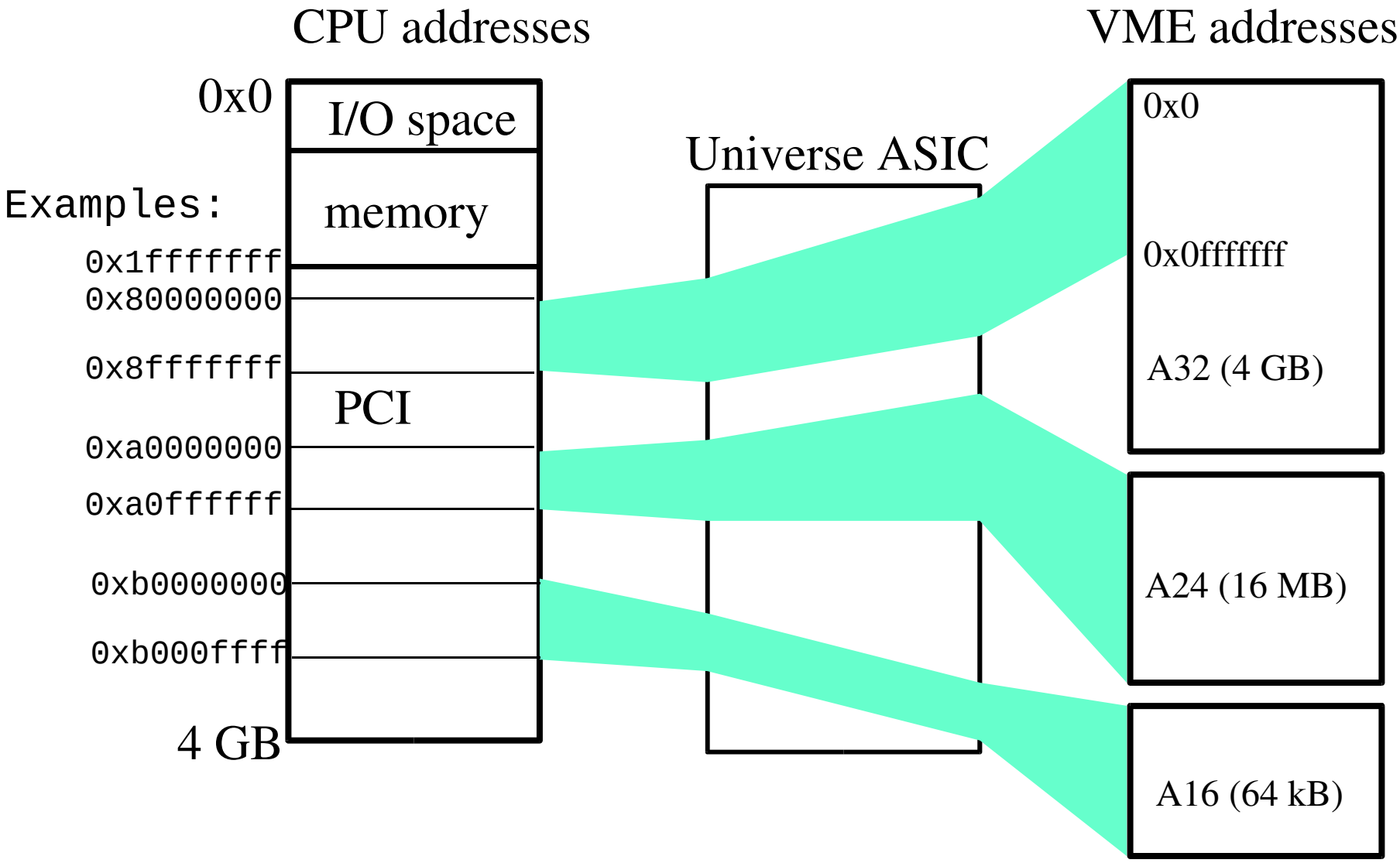
- Usually this is the only master and interrupt handler in the crate
- It often also provides the arbiter functionality (and should therefore be installed in slot 1, despite what is said about cooling)
- It behaves like a normal PC
  - Operating system: Linux, (LynxOS, Windows)
  - Development tools: gcc, g++, gdb
  - Environment: Shell, Xterm, vi, emacs
  - Accessed via: RS232, Ethernet, (VGA)
- It interfaces to VMEbus via a PCI device
  - Typically Tundra Universe
  - Depending on the model and the S/W used it has to be configured in the BIOS or at start-up by special programs
- The PowerPC CPU does instruction reordering. Use the “eieio” assembler instruction to enforce the proper order of execution
- Some SBCs can be equipped with mezzanines (PMC, IP) but this is another story



Debugging tools (2)

- H/W
  - VMEtro VBT325 bus analyzer
    - Stores up to 16000 VMEbus cycles
    - Powerful trigger and sequencer
    - Supports protocol analysis
    - To operate it you need a VT100 (Falco) terminal or a PC with a terminal program (e.g. HypeTerm, minicom, kermit)
    - Can be rented at the El. Pool
  - CES VMDIS8004
    - Low cost bus monitor. Displays the most recent cycle
    - Can latch the first cycle with a bus error or an interrupt
    - Has a built in arbiter (useful if SBC runs hot in slot 1)
    - Can be rented at the El. Pool

Address spaces



Memory map of the VME interface Board

	Address (H)	Master Block Transfer Contr. Regs
Region 0	3FC0 0000	Semaphore Test & Set reg (R only)
	3FC0 0004	Transfer kenath Multipler 0 reg.
	3FC0 0008	Transfer kenath Multipler 1 reg.
	3FC0 000C	Transfer type reg
	3FC0 0010	Local Starting Addr. & GO reg
	3FC0 0014	VME Starting Addr. Reg
	3FC0 0018	A40/A64 Upper Addr. Reg
	3FCO 001C	Master Block Status ID & Intr. Enable
	3FC4 0000	INT Status reg (R only) (xxxx..xxxx ooooS3S2S1S0) (last byte)
	3FC4 0004	LPRPint Status reg (R only)
	3FC8 0000	Control register (W-only) 9-bits NC,NC, Brdsel2, Brdsel1, Brdsel0, F3F2F1F0
	3FCC 0000 3FCC FFFF	Channel board A32/D32 (R/W)
	3FD0 0000 3FD0 FFFF	Channel board A32/D64 block read
	3F4 0000 3FF7 FFFF	NVRAM 32x8bit (R/W) AM 3D
	3FF8 0000 3FFB 7FFF	NVROM 32x8bit (R/W) 32bit mode AM=09